CLAIMS

What is claimed is:

1. A method for processing an instruction within a processor, the method comprising:

executing an instruction within the processor; and

in response to completion of the executed instruction, automatically writing by the processor an instruction disposition value to a register or to a memory buffer, wherein the instruction disposition value indicates whether results from the executed instruction were committed.

2. The method of claim 1 wherein the instruction disposition value is correlated with a predicate value for the executed instruction.

3. The method of claim 2 further comprising:

reading the predicate value from a predicate register that was used for a predication operation while the instruction was executing.

4. The method of claim 1 further comprising:

determining whether or not an enable flag was previously set prior to writing the instruction disposition value.

5. The method of claim 1 further comprising:

reading a memory buffer pointer register within the processor to obtain a pointer to the memory buffer.

6. The method of claim 1 further comprising:

writing a memory address for the memory buffer to a memory buffer pointer register within the processor.

7. The method of claim 1 further comprising:

reading the register or the memory buffer by tracing software to obtain an instruction disposition value; and

writing the instruction disposition value to persistent storage.

8. A method for processing an instruction within a processor, wherein the processor has at least one predicate register, the method comprising:

executing an instruction within the processor; and

if the instruction is controlled by a predicate register, automatically writing by the processor to a register or to a memory buffer a value of the predicate register while executing the instruction in response to completion of the executed instruction.

9. The method of claim 8 further comprising:

if the instruction is not controlled by a predicate register, automatically writing by the processor to a register or to a memory buffer a value that indicates that the instruction was fully executed.

10. The method of claim 8 further comprising:

storing a series of values in the register or the memory buffer for a series of instructions.

11. A processor that performs operations specified by instructions fetched from a memory, the processor comprising:

means for fetching instructions from memory;

means for executing an instruction within the processor; and

means for automatically writing by the processor an instruction disposition value to a register or to a memory buffer in response to completion of the executed instruction, wherein the instruction disposition value indicates whether results from the executed instruction were committed.

12. The processor of claim 11 wherein the instruction disposition value is correlated with a predicate value for the executed instruction.

13. The processor of claim 12 further comprising:

means for reading the predicate value from a predicate register that was used for a predication operation while the instruction was executing.

14. The processor of claim 11 further comprising:

means for determining whether or not an enable flag was previously set prior to writing the instruction disposition value.

15. The processor of claim 11 further comprising:

means for reading a memory buffer pointer register within the processor to obtain a pointer to the memory buffer.

16. The processor of claim 11 further comprising:

means for writing a memory address for the memory buffer to a memory buffer pointer register within the processor.

17. The processor of claim 11 further comprising:

means for reading the register or the memory buffer to obtain an instruction disposition value; and

means for writing the instruction disposition value to persistent storage.

18. A processor that performs operations specified by instructions fetched from a memory, the processor comprising:

means for executing an instruction within the processor; and

means for automatically writing by the processor to a register or to a memory buffer a value of the predicate register while executing the instruction in response to completion of the executed instruction if the instruction is controlled by a predicate register.

19. The processor of claim 18 further comprising:

means for automatically writing by the processor to a register or to a memory buffer a value that indicates that the instruction was fully executed if the instruction is not controlled by a predicate register.

20. The processor of claim 18 further comprising:

means for storing a series of values in the register or the memory buffer for a series of instructions.

21. A data processing system comprising:

means for enabling tracing of a process within the data processing system;

means for executing an instruction within the processor;

means for automatically writing by the processor an instruction disposition value to a register or to a memory buffer in response to completion of the executed instruction, wherein the instruction disposition value indicates whether results from the executed instruction were committed; and

means for storing tracing information.

22. The system of claim 21 wherein the instruction disposition value is correlated with a predicate value for the executed instruction.

23. The system of claim 22 further comprising:

means for reading the predicate value from a predicate register that was used for a predication operation while the instruction was executing.

24. The system of claim 21 further comprising:

means for determining whether or not an enable flag was previously set prior to writing the instruction disposition value.

25. The system of claim 21 further comprising:

means for reading a memory buffer pointer register within the processor to obtain a pointer to the memory buffer.

26. The system of claim 21 further comprising:

means for writing a memory address for the memory buffer to a memory buffer pointer register within the processor.

27. The system of claim 21 further comprising:

means for reading the register or the memory buffer to obtain an instruction disposition value; and

means for writing the instruction disposition value to persistent storage.

28. A computer program product in a computer-readable medium for use in a processor, the computer program product comprising:

means for executing an instruction within the processor; and

means for automatically writing by the processor an instruction disposition value to a register or to a memory buffer in response to completion of the executed instruction, wherein the instruction disposition value indicates whether results from the executed instruction were committed.

29. The computer program product of claim 28 wherein the instruction disposition value is correlated with a predicate value for the executed instruction.

30. The computer program product of claim 28 further comprising:

means for reading the predicate value from a predicate register that was used for a predication operation while the instruction was executing.

31. The computer program product of claim 28 further comprising:

means for determining whether or not an enable flag was previously set prior to writing the instruction disposition value.

32. The computer program product of claim 28 further comprising:

means for reading a memory buffer pointer register within the processor to obtain a pointer to the memory buffer.

33. The computer program product of claim 28 further comprising:

means for writing a memory address for the memory buffer to a memory buffer pointer register within the processor.

34. The computer program product of claim 28 further comprising:

means for reading the register or the memory buffer to obtain an instruction disposition value; and

means for writing the instruction disposition value to persistent storage.

35. A computer program product in a computer-readable medium for use in a processor, the computer program product comprising:

means for executing an instruction within the processor; and

means for automatically writing by the processor to a register or to a memory buffer a value of the predicate register while executing the instruction in response to completion of the executed instruction if the instruction is controlled by a predicate register.

36. The computer program product of claim 35 further comprising:

means for automatically writing by the processor to a register or to a memory buffer a value that indicates that the instruction was fully executed if the instruction is not controlled by a predicate register.

37. The computer program product of claim 35 further comprising:

means for storing a series of values in the register or the memory buffer for a series of instructions.